Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A lead frame for use in a chip package, comprising:

a. a central region having a first plurality of sides;

b. a peripheral edge region having a second plurality of sides positioned in spaced relation around said central region;

c. a first set of leads extending from each of said second plurality of sides, each of said first set of leads being partially defined by a first terminal end, first opposing side surfaces each of which extends along a respective first longitudinal axis, and a lower surface that extends in a first plane;

d. a second set of leads extending from said second plurality of sides, each of said second set of leads being partially defined by a second terminal end, second opposing side surfaces each of which extends along a respective second longitudinal axis, and an upper surface that extends in a second plane; and

e. wherein each of said first set of leads are positioned in staggered non-overlapping relation to corresponding ones of said second set of leads such that said first terminal ends are spaced from said second terminal ends by a first predetermined distance, each of said first longitudinal axes are substantially parallel to and spaced from the adjacent ones of said second longitudinal axes by a second predetermined distance, and said first plane is spaced from said second plane by a third predetermined distance.

2. (original) The lead frame according to claim 1, wherein said first set of leads are formed by a mask having resist material arranged to define the pattern of said first set of leads.

3. (original) The lead frame according to claim 1, wherein said second set of leads are formed by a first mask having resist material arranged to define the pattern of said second set of leads.

4. (original) The lead frame according to claim 3, wherein said first set of leads are formed by a second mask having resist material arranged to define the pattern of said first set of leads, said first and second masks being asymmetrical with respect to one another.

5-8. (cancelled)

9. (currently amended) A chip package, comprising:

a. a first set of leads each of which is partially defined by a first terminal end, first opposing side surfaces each of which extends along a respective first longitudinal axis, and a lower surface that extends in a first plane;

b. a second set of leads each of which is partially defined by a second terminal end, second opposing side surfaces each of which extends along a respective second longitudinal axis, and an upper surface that extends in a second plane; and

c. wherein each of said first set of leads are positioned in non-overlapping staggered relation to corresponding ones of said second set of leads such that said first terminal ends are spaced from said second terminal ends by a first predetermined distance, each of said first longitudinal axes are substantially parallel to and spaced from the adjacent ones of said second longitudinal axes by a second predetermined distance, and said first plane is spaced from said second plane by a third predetermined distance.

10. (original) The chip package of claim 9, further comprising a die pad positioned in spaced relation to said first and second sets of leads.

11. (original) The chip package according to claim 10, further comprising a chip having a predetermined number of input/outputs and mounted on said die pad.

12. (original) The chip package according to claim 11, further comprising wire bonds interconnecting said input/outputs of said chip to corresponding ones of said first and second sets of leads.

13. (original) The chip package according to claim 12, further comprising an epoxy resin encapsulating said package leaving a portion of said first and second sets of leads exposed.